Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

1. (Currently amended) A processor, comprising:

a plurality of pipelined functional units for executing instructions;

a scheduler, coupled to the plurality of functional units, programmed for independently mapping instructions, received from at least two separate instruction groups, to at least a portion of the functional units during a first stage;

centralized dispersal logic within the scheduler to deliver the instructions to the at least a portion of the functional units via an operation bus;

wherein the scheduler is programmed to merge and remap a plurality of instruction subgroups, each subgroup from a respective separate instruction group, to at least a portion of functional units, based on functional unit requirements and availability, during a second stage.

2. (Original) The processor of claim 1, wherein the scheduler is programmed to deliver the instructions to the portion of functional units following merging and remapping.

3. (Canceled)

4. (Original) The processor of claim 1, wherein the functional units execute an increased number of instructions operating at a given clock rate.

5. (Original) The processor of claim 1, wherein the instruction groups follow a simultaneous multi-threading structure.

6. (Original) The processor of claim 1, wherein the instruction groups are prioritized to prevent pipeline failures during execution of instructions.

7. (Currently amended) A machine-readable medium having stored thereon a plurality of executable instructions, the plurality of instructions comprising instructions to:

map instructions, received from at least two separate, independent instruction groups, to at least a portion of a plurality of pipelined functional units during a first stage, wherein the instructions are delivered to the at least a portion of the functional units via an operation bus using centralized dispersal logic within a scheduler of a pipeline; and;

merge and remap a plurality of instruction subgroups, each subgroup from a respective separate instruction group, to at least a portion of functional units, based on functional unit requirements and availability, during a second stage.

8. (Original) The medium of claim 7, wherein said instructions include instructions to deliver the instructions to the portion of functional units following merging and remapping.

9. (Canceled)

10. (Original) The medium of claim 7, wherein the instructions include instructions to execute an increased number of instructions at a given clock rate.

11. (Original) The medium of claim 7, wherein the instruction groups follow a simultaneous multi-threading structure.

12. (Original) The medium of claim 7, wherein the instruction groups are prioritized to prevent pipeline failures during execution of instructions.

13. (Currently amended) A method for dispersing instructions to be executed by a processor, comprising: mapping instructions, received from at least two separate, independent instruction groups, to at least a portion of a plurality of pipelined functional units during a first stage; and

merging and remapping a plurality of instruction subgroups, each subgroup from a respective separate instruction group, to at least a portion of functional units, based on functional unit requirements and availability, during a second stage;

wherein the instructions are delivered to the plurality of functional units using centralized dispersal logic within a scheduler of the processor, via an operation bus.

14. (Original) The method of claim 13, further comprising: delivering the

instructions to the portion of functional units following merging and remapping.

15. (Original) The method of claim 13, wherein the step of merging and remapping includes merging and remapping the instructions to the portion of functional units to allow execution of an increased number of instructions at a given clock rate.

16. (Canceled)

17. (Original) The method of claim 13, wherein the instruction groups follow a simultaneous multi-threading structure.

18. (Original) The medium of claim 13, wherein the instruction groups are prioritized to prevent pipeline failures during execution of instructions.